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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

EDK2239

USER MANUAL

FOR H8S/2239
ON-CHIP FLASH MICROCONTROLLER

Preface

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2. START-UP INSTRUCTIONS

2.1. INSTALLING THE EVALUATION DEVELOPMENT KIT (EDK)

Please refer to the quick start guide provided for initial installation of the EDK.

A copy of the quick start guide and other information relating to this EDK at:

http://www.hmse.com/products/edk/support/

Installing the EDK requires power and serial connection to a host computer.

2.2. SERIAL CONNECTION

The serial communications cable for connecting the EDK to a host computer is supplied. The serial cable has 1:1 connectivity.

Figure 2-1 shows how to connect the EDK to a PC or notebook computer equipped with a nine pin D connector.

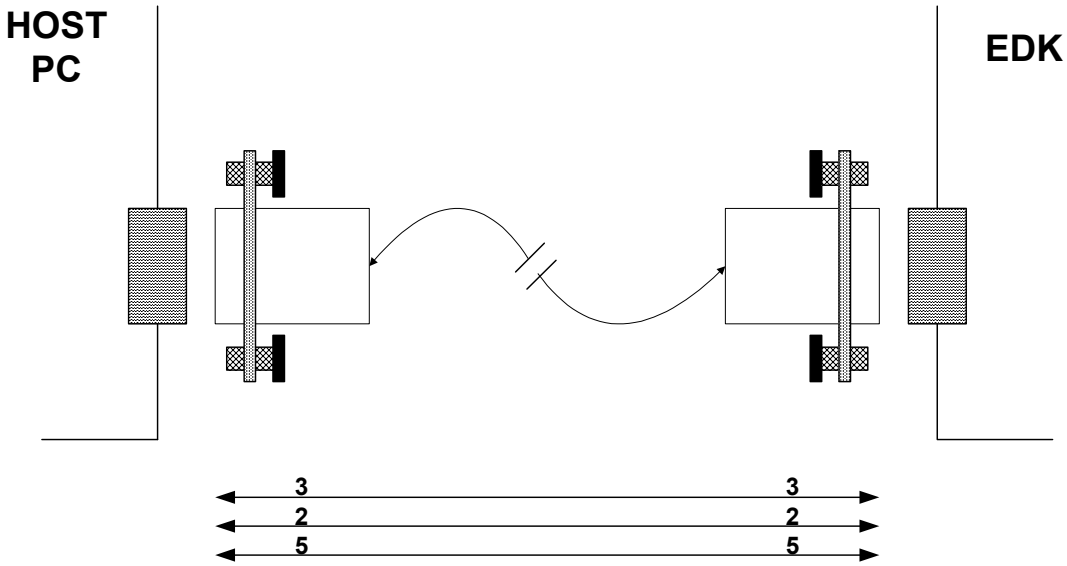


FIGURE 2-1: SERIAL CONNECTION TO PC/NOTEBOOK WITH DB-9 CONNECTOR (SUPPLIED)

2.3. POWER SUPPLY

The EDK hardware requires a power supply of +5V. Since total power consumption can vary widely due to external connections, port states, and memory configuration, use a power supply capable of providing at least 500mA at +5V DC ± 5%.

The design is specified for evaluation of the microcontroller and so does not include circuitry for supply filtering/noise reduction, under voltage protection, over current protection or reversed polarity protection. Caution should be used when selecting and using a power supply.

The power connector on the EDK is a 2.5mm Barrel connector. The center pin is the positive connection.

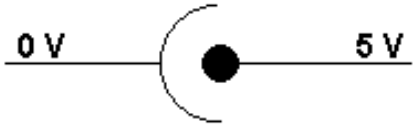


FIGURE 2-2: POWER SUPPLY CONNECTION

Caution: Existing customers using E6000 products note that the polarity of this board is opposite to that for the E6000. Use of the E6000 power supply with this board will damage both board and power supply.

3. EDK BOARD LAYOUT

The diagram shows a general layout of the EDK board.

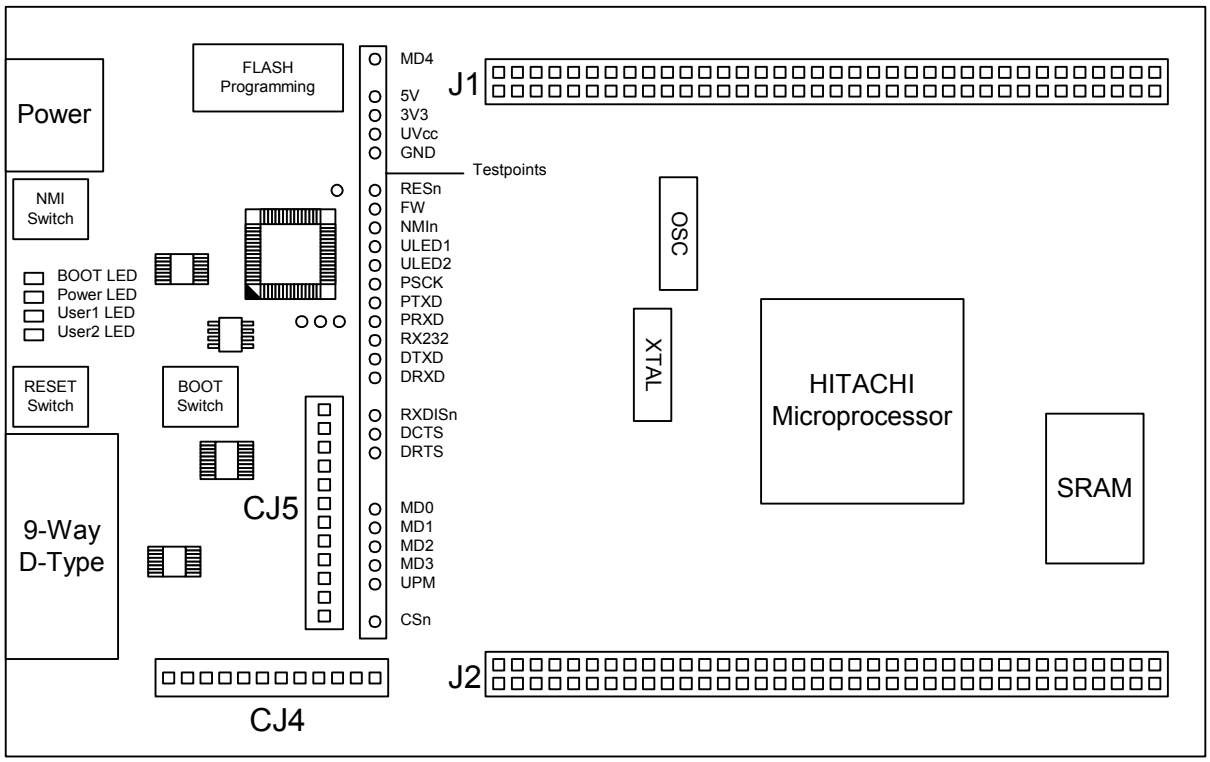


FIGURE 3-1: EDK BOARD LAYOUT

3.1. EDK BLOCK DIAGRAM

The diagram shows the connectivity of the components on the EDK board.

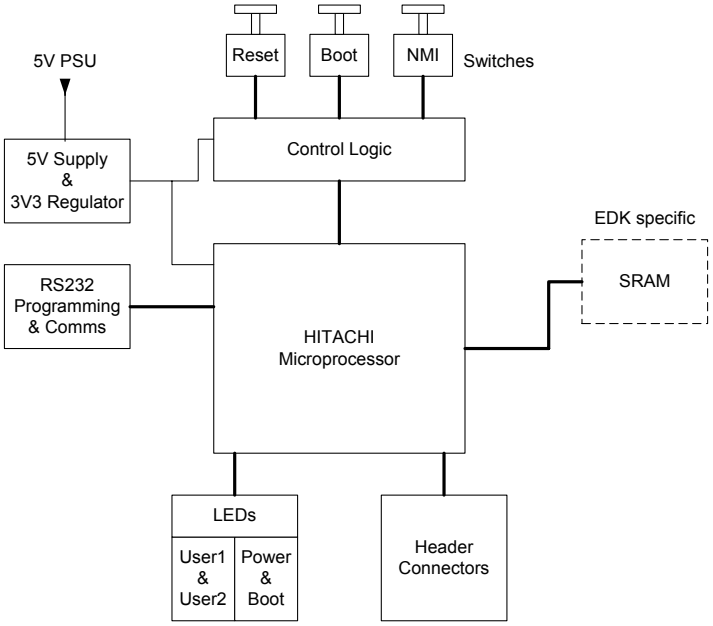


FIGURE 3-2: EDK BLOCK DIAGRAM

4. EDK OPERATION

4.1. USER INTERFACE

The EDK provides three buttons for influencing the operation of the board. The purpose of each button is clearly marked next to it. Refer to the board layout for positions (Section 3)

1. Reset Switch

This button provides the microcontroller with a timed reset pulse of at least 250mS.

2. Boot Switch

This button toggles the operating mode of the microcontroller. A complete description of this function is given in section 5.6.

3. NMI Switch

This button provides a de-bounced signal to the microcontroller for each operation of the button. There is no minimum or maximum activation time for this button.

4.2. SERIAL INTERFACE

The serial interface on the EDK board has several functions. The serial port on the microcontroller directly supports three wire serial interfaces. Options are provided on the board for the user to write handshaking routines using standard port pins. Other board option links allow users to control the entry and exit from boot mode using the same handshaking signals. Refer to section 5 for details on setting serial interface options.

4.2.1. CONNECTOR PIN DEFINITIONS

The EDK RS232 interface conforms to Data Communication Equipment (DCE) format allowing the use of 1-1 cables when connected to Data Terminal Equipment (DTE) such as an IBM PC. The cable used to connect to the EDK will affect the available board options. A fully wired cable can allow handshaking between the microcontroller and the host PC, subject to setting the board options and the availability of suitable host software. Handshaking is not supported as standard on the microcontroller so for normal use a minimal three-wire cable can be used. The minimum connections are unshaded in the following table.

EDK DB9 Connector Pin	Signal	Host DB9 Connector Pin
1	No Connection	1
2	EDK Tx Host Rx	2
3	EDK Rx Host Tx	3
4	No Connection	4
5	Ground	5
6	No Connection	6
7	* EDK CTS Host RTS	7
8	* EDK RTS Host CTS	8
9	No Connection	9

TABLE 4-1: RS232 INTERFACE CONNECTIONS

* These are not connected on the EDK by default. See section 5.4 for more details.

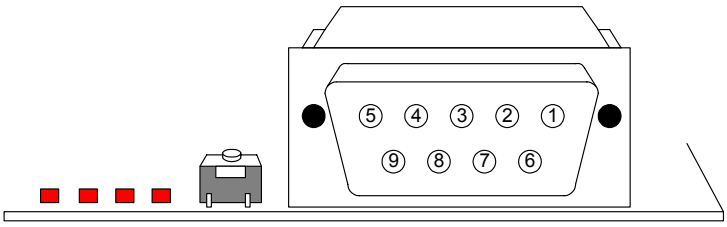


FIGURE 4-1: EDK SERIAL PORT PIN NUMBERING

4.2.2. CRYSTAL CHOICE

The operating crystal frequency has been chosen to support the fastest operation with the fastest serial operating speeds. The value of the crystal is 14.745MHz.

The following table shows the baud rates and Baud Rate Register (BRR) setting required for each communication rate using the above default operating speed. It also confirms the resultant baud rate and the bit error rate that can be expected.

Baud Rate Register Settings for Serial Communication Rates												
SMR Setting:	**0**			**1**			**2**			**3**		
Comm. Baud	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**	**BRR setting**	**Actual Rate**	**ERR (%)**
110	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	64	110.77	0.70
300	invalid	invalid	invalid	invalid	invalid	invalid	95	300	0.00	23	300	0.00
1200	invalid	invalid	invalid	95	1200	0.00	23	1200	0.00	5	1200	0.00
2400	191	2400	0.00	47	2400	0.00	11	2400	0.00	2	2400	0.00
4800	95	4800	0.00	23	4800	0.00	5	4800	0.00	1	3600	-25.00
9600	47	9600	0.00	11	9600	0.00	2	9600	0.00	invalid	Invalid	invalid
19200	23	19200	0.00	5	19200	0.00	1	14400	-25.00	invalid	Invalid	invalid
38400	11	38400	0.00	2	38400	0.00	invalid	invalid	invalid	invalid	invalid	invalid
57600	7	57600	0.00	1	57600	0.00	invalid	invalid	invalid	invalid	invalid	invalid
115200	3	115200	0.00	0	115200	0.00	invalid	invalid	invalid	invalid	invalid	invalid
230400*	1	230400	0.00	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid
460800*	0	460800	0.00	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid	invalid

TABLE 4-2 CRYSTAL FREQUENCIES FOR RS232 COMMUNICATION

** Note: The device used to convert the RS232 serial information to logic signals for the microcontroller is limited to 120kBaud. The rates above this level can only be utilised if the user provides direct logic level communications.*

The user may replace the HC49/U surface mounted AT cut crystal with another of similar type within the operating frequency of the microcontroller device. Please refer to the hardware manual for the microcontroller for the valid operating range.

Alternatively the user may fit an oscillator module – or provide an external clock source. When providing an oscillator module or external source it is highly recommended that the load capacitors for the AT crystal are removed from the PCB. These are physically placed within the PCB outline of the oscillator module for easy location and to ensure they are removed when using this option.

When changing the crystal frequency the pre-loaded debugging monitor will not function. In this situation the user is responsible for providing code to evaluate the device away from the default operating speed.

4.2.3. REMOVABLE COMPONENT INFORMATION.

This information is provided to allow the replacement of components removed from the board as described in section 4.2.2.

Component	Cct. Ref	Value	Rating	Manufacturer
Load Resistor (X2)	R8	1MΩ	0805 1%	Welwyn WCR Series
Load Resistor (X3)	R7	1MΩ	0805 1%	Welwyn WCR Series
Load capacitors (X2)	C1,C2	22pF	0603 10% 25V	AVX 0603 3 A 220 KAT
Load capacitors (X3)	C3,C4	15pF	0603 10% 25V	AVX 0603 3 A 150 KAT

TABLE 4-3: REMOVABLE COMPONENT INFORMATION

Care must be taken not to damage the tracking around these components. Only use soldering equipment designed for surface mount assembly and rework.

4.3. SRAM

Provision has been made for a 4MBit SRAM device on the board, allowing 256kx16 operation.

Please refer to the schematic for details of the components to be fitted for external SRAM functionality.

SCI2, used as the default serial port for the EDK, shares the upper two address lines (A17 & A18). These may be isolated from the SRAM by not fitting 0R links (R20 & R23), and pulling up the address lines on the SRAM using 4K7 resistors (R21 & R22). This allows for a (64k x 16) configuration.

Alternatively the device may be programmed using SCI2, but configured to use the debug serial port (SCI0), as detailed in section 5.4, for access to the full address range (256k x 16).

The SRAM, (when fitted), is connected to Chip Select 1 (CS1), which can address the range H200000 – H27FFFF. The usable address range without modifying the board jumpers mentioned, is H'200000 – H'21FFFF.

4.4. MEMORY MAP

Table 4-4 illustrates the EDK memory map for mode 6.

Section Start Section End	Section Allocation
H'0000 0000	On-Chip ROM
H'0005 FFFF	
H'0006 0000	RESERVED
H'001F FFFF	
H'0020 0000	SRAM (A1-A18) Area 1 (controlled by CS1)
H'0027 FFFF	
H'0028 0000	RESERVED
H'00FF 6FFF	
H'00FF 7000	On-Chip RAM
H'00FF EFBF	
H'00FF EFC0	RESERVED
H'FFFF F7FF	
H'FFFF F800	Internal I/O Registers
H'FFFF FF3F	
H'FFFF FF40	RESERVED
H'FFFF FF5F	
H'FFFF FF60	Internal I/O Registers
H'FFFF FFBF	
H'FFFF FFC0	On-Chip RAM
H'FFFF FFFF	

TABLE 4-4: MEMORY MAP (DEFAULT MODE 2)

4.5. SRAM ACCESS TIMING

External access timing is defined by several registers, allowing different types of devices to be addressed. The registers for the selection of wait states and signal extensions are given below with recommended values for the EDK.

Register	Address	Recommended Setting for EDK	Function
ABWCR	FFFED0	H'FD	Enables 16-bit access to area 1
ASTCR	FFFED1	H'FF	3-State access
WCRH	FFFED2	H'FF	3-Wait state access
WCRL	FFFED3	H'FF	3-Wait state access
PFCR	FFFDEB	H'09	Enables A16 to A8 (used when SCI2.is used)
PFCR	FFFDEB	H'0B	Enables A18 to A8 (used when SCI2.is not used)

TABLE 4-5: SRAM ACCESS CONTROL REGISTERS

Please refer to the hardware manual for the microcontroller for more information on these register settings.

4.6. LEDS

The EDK has four red LEDs. The function of each LED is clearly marked on the silk screen of the PCB. Please refer to the board layout diagram for position information (Section 3).

When the board is connected to a power source the Power (PWR) led will illuminate. The Boot mode indication LED will illuminate when the microcontroller has been placed into Boot mode. Please see section 2 for more details of this function.

There are two LEDs dedicated for user control these are marked USR1 and USR2. Each LED will illuminate when the port pin is in a logical high state.

The user LEDs are connected to the following ports:

LED Identifier	Port Pin	Microcontroller Pin	Pin Functions on Port Pin
USR1	P10	34	P10/TIOCA0/DACK0n/A20
USR2	P11	35	P11TIOCB/DACK1/A21

TABLE 4-6: LED PORT CONNECTIONS

5. BOARD OPTIONS

The EDK has a number of configuration settings set by jumpers CJ4 (A, B, C, D) CJ5 (A, B, C, D) and zero-ohm links. Common EDK functions can be set using the jumpers as described in sections 5.3 and 5.2. The additional zero-ohm links provide additional features that may be required to interface with other systems.

All the Jumper link settings are three pin options. There are four sets of options on each header.

The headers are numbered from 1 to 12 with pin 1 marked on the PCB by an arrow pointing to the pin. The diagram below shows the numbering of these jumper links and indicates jumpers fitted 1-2 for each three-pin jumper.

5.1. JUMPER LINKS

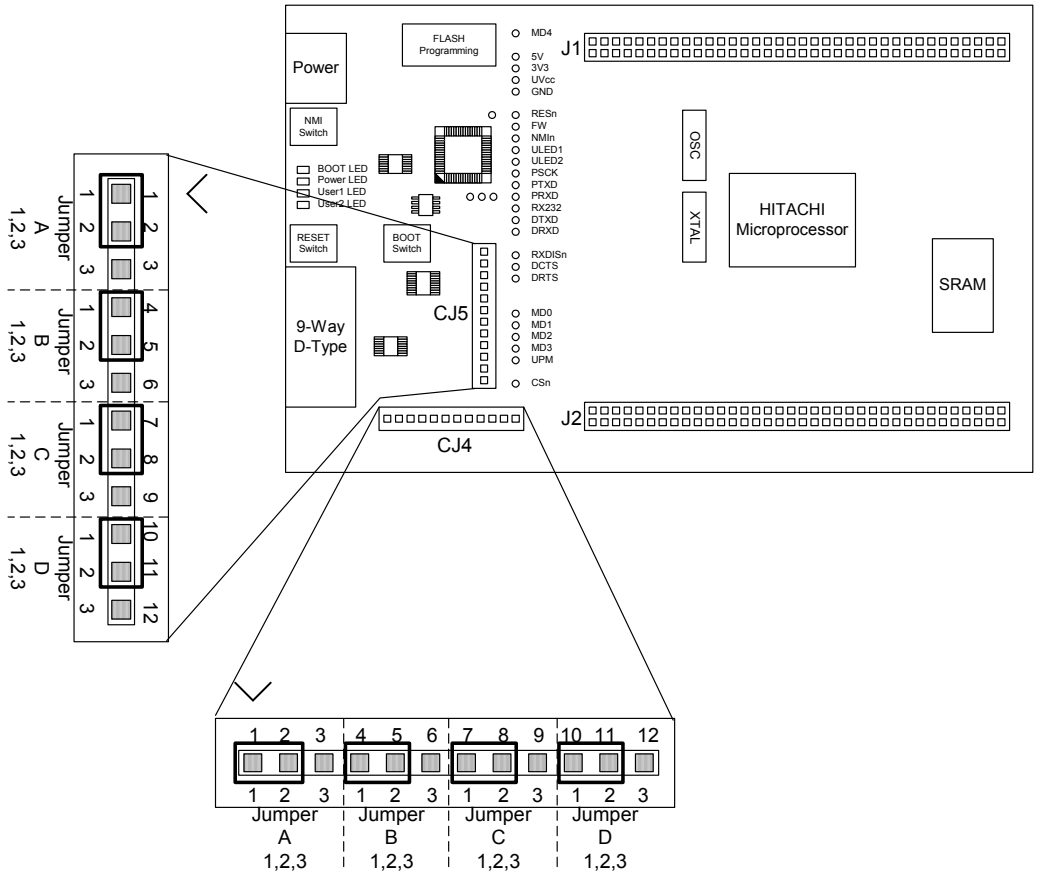


FIGURE 5-1: JUMPER CONFIGURATION

The following tables define each jumper and its settings.

5.2. USER MODE SETTINGS – CJ5

CJ5 is used to set the operating mode of the microcontroller.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 5-A Default 2-3	User Mode Setting Bit 0	MD0 pulled High	**MD0 pulled Low**
CJ 5-B Default 1-2	User Mode Setting Bit 1	**MD1 pulled High**	MD1 pulled Low
CJ 5-C Default 2-3	User Mode Setting Bit 2	**MD2 pulled High**	MD2 pulled Low
CJ 5-D Default 1-2	User Mode Setting Bit 3	**MD3 pulled High**	MD3 pulled Low

TABLE 5-1: USER MODE: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

The default settings indicated in bold text place the microcontroller into Mode 6.

5.3. EDK OPTIONS – CJ4

The EDK options provide access to commonly used features of the EDK range.

These jumpers must be fitted at all times to ensure correct operation of the EDK.

Jumper	Function	Setting 1-2	Setting 2-3
CJ 4-A Default 2-3	Serial Receive Source	Disables the RS232 receive signal to enable the use of the Flash Programming Header	**Enables the RS232 receive signal. The Flash Programming Header* must not be used in this state.**
CJ 4-B Default 2-3	User Programming Mode	Disables the Flash write hardware protection. The flash can be overwritten in User Mode.	**Enables the Flash write hardware protection. The flash cannot be overwritten in User Mode.**
CJ 4-C Default 2-3	Chip select Enable	Connect CSn of the SRAM to PG3 of the H8S/2239	**Isolate and pull high, CSn of the SRAM**
CJ 4-D Not Fitted	Not Used		

TABLE 5-2: BOARD OPTION: JUMPER SETTINGS (DEFAULT SETTINGS IN BOLD)

*See section 5.5

The following table lists the connections to each jumper pin.

Pin	Net Name	Description
1	UVCC	Microcontroller Supply Voltage
2	RXDISn	Disable Flash Header functions. Pulled low. (Enables RX232)
3	No Connection	No Connection
4	UVCC	Microcontroller Supply Voltage
5	UPM	CPLD Controlled option to set Flash Write (FW). Pulled low.
6	No Connection	No Connection
7	PG3	Port G3 of the H8S/2239 (CS1)
8	CSn	Chip select of the SRAM, and a 4K7 pull up.
9	No Connection	No Connection
10	No Connection	No Connection
11	No Connection	No Connection
12	No Connection	No Connection

5.4. SERIAL PORT SELECTION

The programming serial port is connected to the RS232 connector by default. This allows direct programming of the EDK using the supplied software tools. A secondary serial port is available on the microcontroller and can be connected to the RS232 connector by changing some board option links. The additional port option allows the user to write messages or connect to other devices via the serial port while programming support is provided by the Flash programming header.

The following surface mount, zero-ohm link settings are fitted by default and connect the RS232 header to the programming serial port of the microcontroller.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Fitted	Transmit data from EDK	PA1
CR23	Fitted	Receive data to EDK	PA2
CR19	Not Fitted	Alternate Transmit data from EDK	P30
CR22	Not Fitted	Alternate Receive data to EDK	P31

TABLE 5-3: OPTION LINKS – DEFAULT SETTINGS

To enable the use of this alternate port the user must change the settings to those in the following table.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR20	Not Fitted	Transmit data from EDK	PA1
CR23	Not Fitted	Receive data to EDK	PA2
CR19	Fitted	Alternate Transmit data from EDK	P30
CR22	Fitted	Alternate Receive data to EDK	P31

TABLE 5-4: OPTION LINKS – ALTERNATE SERIAL PORT

The user may implement a handshaking protocol on the EDK. This is not supported with the software tools supplied. To support this option two spare port pins have been allocated on the microcontroller. Using these port pins the CTS and RTS lines of the host serial interface can be controlled.

The user may also control the operation of the board via the same handshaking lines. This is not supported with the software tools supplied but may be written by the user. Using the CTS line the user may simulate pressing the boot button, see section:5.6. This will cause the EDK to swap into and out of Boot mode on each low-level activation of CTS. Feedback of the current mode is provided on the RTS line. A high level indicates boot mode and a low level indicates user mode.

The following settings are made by default, and ensure that there are no conflicts on unnecessary microcontroller pins.

Zero-ohm Link ID	Default	Function	Microcontroller Port Pin
CR12	Not Fitted	Mode State out from EDK	N/A (From CPLD*)
CR7	Not Fitted	Change Mode request to EDK	N/A (From CPLD*)
CR16	Not Fitted	Alternate RTS232 – Ready to send – from EDK	P15
CR13	Not Fitted	Alternate CTS232 – Clear to send – to EDK	P14

TABLE 5-5: OPTION LINKS – SERIAL PORT CONTROL

* See section 5.6

Note: These setting pairs are exclusive:
If CR12 and CR7 are fitted; CR16 and CR13 must not be fitted.
If CR16 and CR13 are fitted; CR12 and CR7 must not be fitted.

5.5. FLASH PROGRAMMING HEADER

The Flash Programming header is used with the Hitachi Flash Debug Board (FDB). The FDB is a USB based programming tool for control and programming of Hitachi microcontrollers, available separately from Hitachi. This header provides direct access for the FDB to control the EDK microcontroller.

To utilise this header the user must make the following changes to the board configuration.

1. Disable the RX232 signal from the RS232 transceiver.
   Jumper link CJ4-A is provided for this purpose. Please refer to section5.3.
2. Disable User Program Mode using jumper CJ4-B. Please refer to section5.3.

Caution: Do not operate the board with the user mode jumpers removed and the FDB disconnected, as the microcontroller mode pins will float to an indeterminate state. This may damage the microcontroller device.

5.6. BOOT CONTROL

The method for placing the microcontroller device in to Boot mode for reprogramming has been incorporated into a complex programmable logic device (CPLD). This is not necessary for most user designs but allows a measure of increased flexibility for the EDK designs. Mode transitions including boot mode transitions only require the reset to be held active while the mode settings are presented. On releasing reset the microcontroller will be in the required mode.

The logic design detects a power up event and provides a timed reset pulse to guarantee the reset of the device. At the end of the rest pulse the processor will be placed in user mode and any code in the device will execute.

During user mode the NMI button can be pressed at any time. This will provide a single de-bounced NMI interrupt to the device.

Pressing the boot button will cause the boot mode controller to reset the device and, during the reset period, present the required mode settings to start the device in boot mode. At the end of the reset period the boot mode settings will have been latched into the device, which will then be ready to accept a boot mode connection via the RS232 interface or the flash programming header. Pressing the boot button during a normal reset will not cause the EDK to enter boot mode.

The boot mode settings are fixed at mode 2. The required mode settings are made using a tri-state capable buffer.

Note: The boot control device is programmed to support all possible EDK products.
For this reason the reset pulse is over 500ms. Repetitive activation of either the Boot or Reset buttons will restart the reset timer and extend the reset period. Pressing the boot button within the 500mS period of a reset will not cause the board to enter boot mode.

5.6.1. CPLD CODE

The code is based upon a four state machine providing a guaranteed reset period, which can be extended by holding the relevant control input in the active state. When released the timer will extend the reset for approximately 500mS.

The states are split into two functions, one for User mode and one for Boot mode. The first state of each is used to hold the reset line active. When the timer expires then the second state is used to hold the device in the selected mode and wait for an external control signal to either move back into the user reset state or into the boot reset state.

5.6.2. STATE DIAGRAM

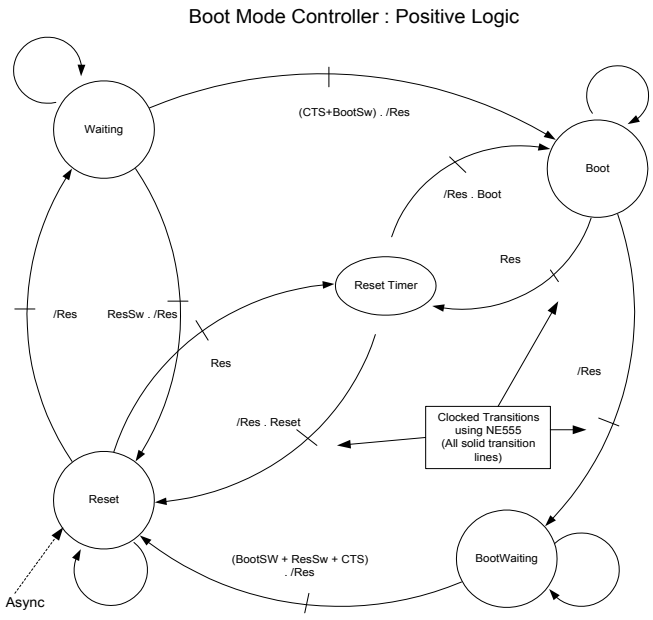


FIGURE 5-2: CPLD STATE DIAGRAM

6. MICROCONTROLLER HEADER CONNECTIONS

The following table lists the connections to each or the headers on the board.

6.1. HEADER J1

J1							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	STBY	STBYn	61	2	VCC	UVCC	62
3	RES	RESn	59	4	NMI	NMIn	60
5	OSC2	CON_OSC2	57	6	OSC1	CON_OSC1	58
7	MD0	MD0	55	8	MD1	MD1	56
9	Vref	CON_Vref	53	10	AVCC	CON_AVCC	54
11	P41/AN1	P41	51	12	P40/AN0	P40	52
13	P43/AN3	P43	49	14	P42/AN2	P42	50
15	P45/AN5	P45	47	16	P44/AN4	P44	48
17	P47/AN7	P47	45	18	P46/AN6	P46	46
19	P97/DA1	P97	43	20	P96/DA0	P96	44
21	P17/TIOCB2/TCLKD	P17	41	22	AVSS	CON_AVSS	42
23	P15/TIOCB1/TCLKC	DRTS	39	24	P16/TIOCA2/IRQ1	P16	40
25	P13/TIOCD0/TCLKB/ A23	P13	37	26	P14/TIOCA1/IRQ0	DCTS	38
27	P11/TIOCB0/DACK1/ A21	ULED2	35	28	P12/TIOCC0/TCLKA/A 22	P12	36
29	PA3/A19/SCK2	PSCK	33	30	P10/TIOCA0/DACK0/A 20	ULED1	34
31	PA1/A17/TxD2	PTXD	31	32	PA2/A18/RxD2	PRXD	32
33	PB7/A15/TIOCB5	PB7	29	34	PA0/A16	PA0	30
35	PB5/A13/TIOCB4	PB5	27	36	PB6/A14/TIOCA5	PB6	28
37	PB3/A11/TIOCD3	PB3	25	38	PB4/A12/TIOCA4	PB4	26
39	PB1/A9/TIOCB3	PB1	23	40	PB2/A10/TIOCC3	PB2	24
41	PC7/A7	PC7	21	42	PB0/A8/TIOCA3	PB0	22
43	PC5/A5	PC5	19	44	PC6/A6	PC6	20
45	PC3/A3	PC3	17	46	PC4/A4	PC4	18
47	PC1/A1	PC1	15	48	PC2/A2	PC2	16
49	PC0/A0	PC0	13	50	VSS	Ground	14

6.2. HEADER J2

J2							
Pin No	**Function**	**EDK Symbol**	**Device pin**	**Pin No**	**Function**	**EDK Symbol**	**Device pin**
1	XTAL	CON_XTAL	63	2	VSS	Ground	64
3	EXTAL	CON_EXTAL	65	4	FWE	FW	66
5	MD2	MD2	67	6	PF7/ø	PF7	68
7	PF6/AS	PF6	69	8	PF5/RD	PF5	70
9	PF4/HWR	PF4	71	10	PF3/LWR/IRQ3/ADTRG	PF3	72
11	PF2/WAIT	PF2	73	12	PF1/BACK/BUZZ	PF1	74
13	PF0/BREQ/IRQ2	PF0	75	14	P30/TxD0	DTxD	76
15	P31/RxD0	DRxD	77	16	P32/SCK0/SDA1/IRQ4	P32	78
17	P33/TxD1/SCL1	P33	79	18	P34/RxD1/SDA0	P34	80
19	P35/SCK1/SCL0/IRQ5	P35	81	20	P36	P36	82
21	P77/TxD3	P77	83	22	P76/RxD3	P76	84
23	P75/TMO3/SCK3	P75	85	24	P74/TMO2/MRES	P74	86
25	P73/TMO1/TEND1/CS7	P73	87	26	P72/TMO0/TEND0/CS6	P72	88
27	P71/TMRI23/TMCI23/DREQ1/CS5	P71	89	28	P70/TMRI01/TMCI01/DREQ0/CS4	P70	90
29	PG0/IRQ6	PG0	91	30	PG1/CS3/IRQ7	PG1	92
31	PG2/CS2	PG2	93	32	PG3/CS1	PG3	94
33	PG4/CS0	PG4	95	34	PE0/D0	PE0	96
35	PE1/D1	PE1	97	36	PE2/D2	PE2	98
37	PE3/D3	PE3	99	38	PE4/D4	PE4	100
39	PE5/D5	PE5	1	40	PE6/D6	PE6	2
41	PE7/D7	PE7	3	42	D8/PD0	PD0	4
43	D9/PD1	PD1	5	44	D10/PD2	PD2	6
45	D11/PD3	PD3	7	46	D12/PD4	PD4	8
47	D13/PD5	PD5	9	48	D14/PD6	PD6	10
49	D15/PD7	PD7	11	50	CVCC	NC12	12

7. CODE DEVELOPMENT

7.1. HMON

7.1.1. MODE SUPPORT

The HMON library is built to support Advanced Expanded Mode only. The Device supports Modes 6 and 7.

7.1.2. BREAKPOINT SUPPORT

The monitor utilises the PC Break Controller for code located in ROM, allowing a single breakpoint to be set in the code. Code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM.

7.1.2.1. CODE LOCATED IN FLASH / ROM

Double clicking in the breakpoint column in the code sets the breakpoint. Adding a further breakpoint elsewhere in the code removes the previous one.

7.1.2.2. CODE LOCATED IN RAM

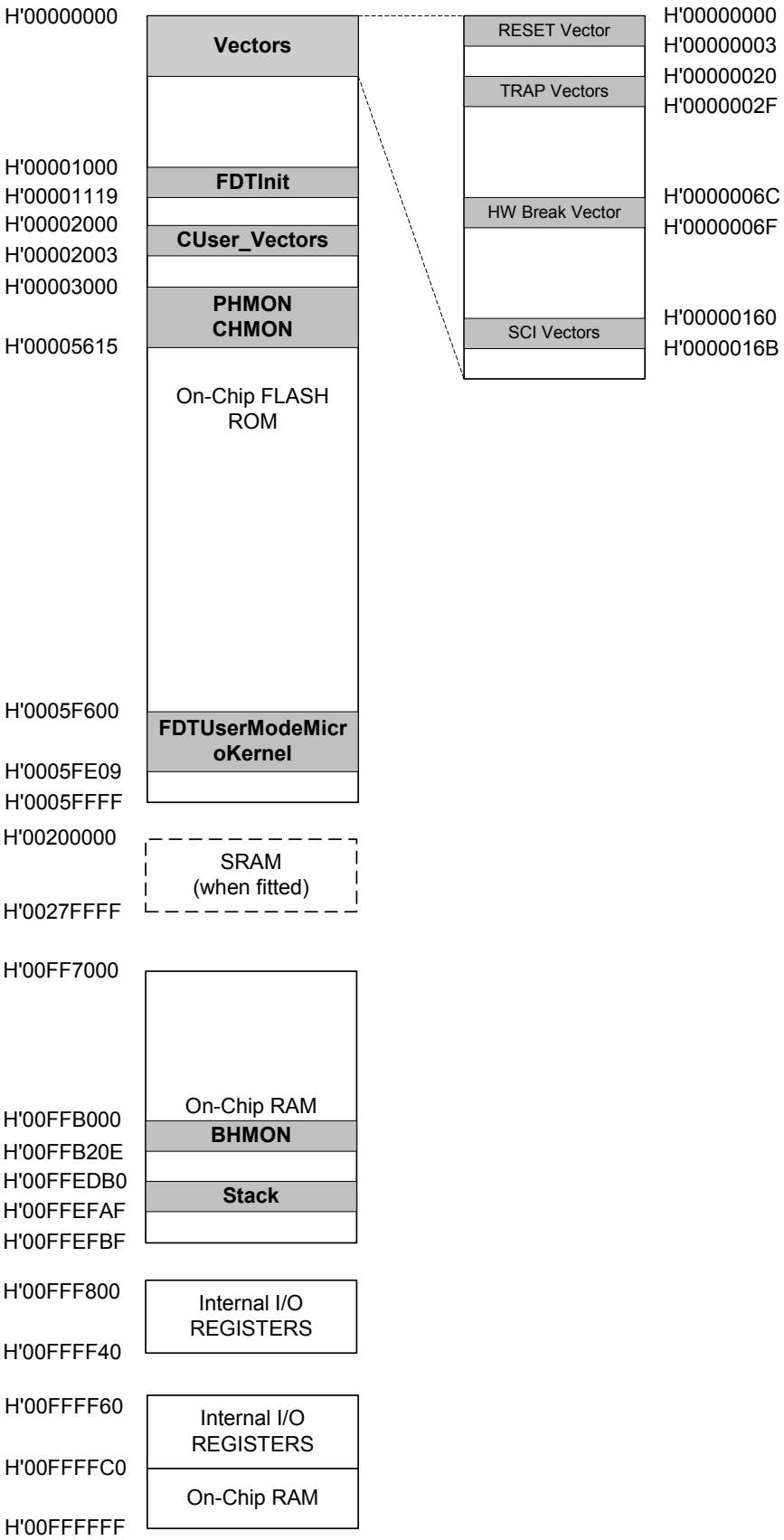
Double clicking in the breakpoint column in the code sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them.

7.1.3. HMON CODE SIZE

HMON is built along with the debug code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start Location	Size (H'bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0) Required for Startup of HMON	H' 000000000	4
TRAP_VECTORS	Trap Vectors (Vector 8, 9, 10, 11) Required by HMON to create Trap Breakpoints in RAM	H' 00000020	10
HW_BREAK_VECTORS	HMON Break Controller (Vector 27) Required by HMON to create Breakpoints in ROM	H' 0000006C	4
SCI_VECTORS	HMON Serial Port Vectors (Vector 88, 89, 90) Used by HMON when EDK is configured to connect to the default serial port.	H' 00000160	C
PHMON	HMON Code	H' 00003000	24CE
CHMON	HMON Constant Data	H' 000054CE	148
BHMON	HMON Uninitialised data	H' 00FFB000	20F
FDTInit	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 00001000	11A
FDTUserModeMicroKernel	FDT User Mode Kernel. This is at a fixed location and must not be moved. Should the kernel need to be moved it must be re-compiled.	H' 0005F600	80A
CUser_Vectors	Pointer used by HMON to point to the start of user code. This is at a fixed location and must not be moved for the Reset CPU, and Go Reset commands to function.	H' 00002000	4

7.1.4. MEMORY MAP



7.1.5. BAUD RATE SETTING

HMON has initially set to connect at 115200Baud. Should the user wish to change this, the value for the BRR in HMONserialconfiguser.c will need to be changed and the project re-built. Please refer to the HMON User Manual for further information.

7.1.6. INTERRUPT MASK SECTIONS

HMON has an interrupt priority of 6. The serial port has an interrupt priority of 7. Modules using interrupts should be set to lower than this value (6 or below), so that serial communications and debugging capability is maintained.

7.2. ADDITIONAL INFORMATION

For details on how to use Hitachi Embedded Workshop (HEW), with HMON, `refer to the HEW manual available on the CD or from the web site.

For information about the H8S/2239 series microcontrollers refer to the H8S/2239 *Series Hardware Manual*

For information about the H8S/2239 assembly language, refer to the H8S *Series Programming Manual*

Further information available for this product can be found on the HMSE web site at:

http://www.hmse.com/products/support.htm

General information on Hitachi Microcontrollers can be found at the following URLs.

Global: www.hitachisemiconductor.com

Europe: www.hmse.com